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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 7 : G06T

A2

(11) International Publication Number: **WO 00/30033**

(43) International Publication Date: 25 May 2000 (25.05.00)

(21) International Application Number: PCT/US99/27449

(22) International Filing Date: 17 November 1999 (17.11.99)

(30) Priority Data:
60/108,784 17 November 1998 (17.11.98) US

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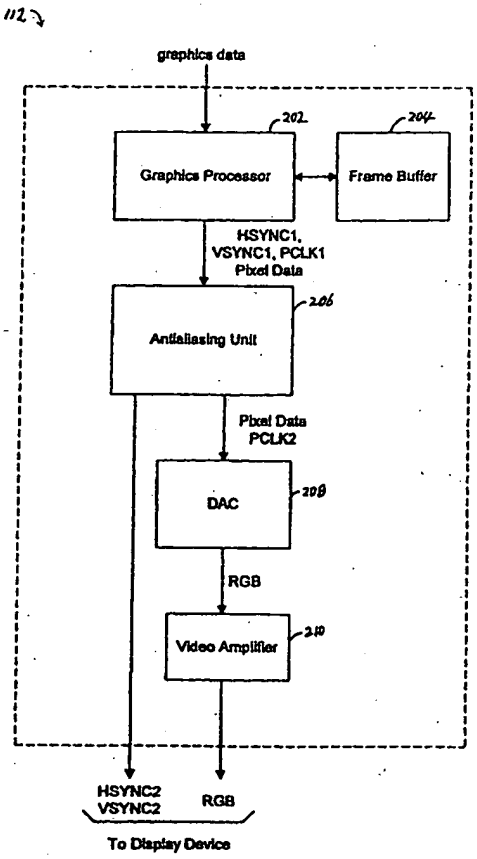
(81) Designated States: AE, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CR, CU, CZ, DE, DK, DM, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

Published
Without international search report and to be republished upon receipt of that report.

(54) Title: DEVICE AND METHOD FOR ANTIALIASING HIGH RESOLUTION PIXEL DATA FOR LOWER RESOLUTION DISPLAY

(57) Abstract

Disclosed is a device and a method for antialiasing high resolution pixel data into low resolution pixel data for display at the low resolution. The high resolution pixel data defines pixel values for a plurality of horizontal scanlines with each scanline being defined by a plurality of the high resolution pixel data. The device includes a horizontal antialiazing unit, a first and a second storage units, and a vertical antialiasing unit. The horizontal antialiasing unit is adapted to sequentially receive the high resolution pixel data and sequentially antialiases N contiguous horizontal pixels associated with M scanlines to generate a set of horizontally antialiased pixel data for the M scanlines. The horizontally antialiased pixel data for the M scanline defines a set of vertically contiguous pixel data. The first and second storage units are capable of receiving and storing the horizontally antialiased pixel data associated with the M scanlines from the horizontal antialiasing unit. One storage unit receives and stores horizontally antialiased pixel data for the next M scanlines as a receiving buffer while the other storage unit provides the horizontally antialiased pixel data as an access buffer for vertical antialiasing. The vertical antialiasing unit is coupled to receive the horizontally–antialiased pixel data associated with the M scanlines from the access buffer. The vertical antialiasing unit performs vertical antialiasing on the vertically contiguous horizontally–antialiased pixel data to generate a pixel value for each NxM set of the high resolution pixel data.



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DEVICE AND METHOD FOR ANTIALIASING HIGH RESOLUTION PIXEL DATA FOR LOWER RESOLUTION DISPLAY

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates generally to antialiasing, and more particularly to antialiasing high resolution graphics data into low resolution pixel data for display.

2. Description of the Related Art

Modern display technology, in both application software and display devices, is driving for ever higher resolutions to achieve clearer and finer image details. Indeed, newer display monitors with higher resolutions driven by latest high resolution computer systems are rapidly displacing older, lower resolution monitors.

If is often said that the processing power of computer systems increases two-fold every 18 months according to the often quoted Moore's Law. Hence, computer systems can become old and obsolete in a matter of months when new applications requiring more processing power are introduced.

In components in computer systems, display monitors often can be used for years longer than the rest of the computer systems. Moreover, monitors are one of the more expensive components in the computer systems and thus represent a substantial investment for most users. Given such an investment value, computer users often upgrade computers by reusing the old monitors with a new computer system. However, some old monitors (e.g., CGA, EGA monitors) are not capable of displaying higher resolutions available in the modern computer systems. Moreover, smaller monitors (e.g., 14" and 15" monitors) typically are not able to display images at high resolutions such as 1024x768.

In computer graphics technology, aliasing refers to distortion or jagged appearance of an object, which is typically caused by undersampling. Antialiasing is a technique that has been used to improve the distorted or jagged appearance of displayed raster lines by increasing the sampling rate. Traditionally, antialiasing has been performed using an accumulation buffer to

hold one or more frames of pixel data. For example, one approach uses the accumulation buffer to accumulate the antialiased pixel values for an entire frame of pixels.

Unfortunately, using the accumulation buffer is costly to implement due to the cost of memory. For example, storing a frame of pixel data at a resolution of 640x480 at 8-bits per R, G, and B pixel components typically requires at least about 0.9 kilobytes (Kbytes) of memory per frame. When the resolution is increased to 800x600, the storage requirement increases to at least 1.4 Megabytes (Mbytes) of memory. For 1024x768 resolution, the memory requirement further increases to about 2.5 Mbytes. In addition, the increase in resolution typically requires more costly supporting circuitry, which adds to the cost of implementing the accumulation buffer.

Another drawback associated with the traditional antialiasing pixel data using an accumulation buffer is a delay introduced by one or more frames accumulated in the accumulation buffer. That is, the storage of a frame in an accumulation buffer translates into a time delay equal to at least the time to accumulate the frame in the buffer. Since the state of the art applications often require real time performance, such a delay may not satisfy the real time processing requirements of these applications.

Thus, what is needed is a device and method for efficiently antialiasing high resolution pixel data for display at a lower resolution without employing a costly accumulation buffer. What is further needed is a device, system, and method that performs such antialiasing without substantial delay so as to meet real time requirements of performance critical applications.

SUMMARY OF THE INVENTION

The present invention fills these needs by providing a device and a method for antialiasing high resolution pixel data for display at a lower resolution. It should be appreciated that the present invention can be implemented in numerous ways, including as a process, an apparatus, a system, a device, a method, or a computer readable medium.

In one embodiment, the present invention provides a device for antialiasing high resolution pixel data into low resolution pixel data for display at the low resolution. The high resolution pixel data defines pixel values for a plurality of horizontal scanlines with each scanline being defined by a plurality of the high resolution pixel data. The device includes a horizontal antialiasing unit, a first and a second storage units, and a vertical antialiasing unit. The horizontal antialiasing unit is adapted to sequentially receive the high resolution pixel data and sequentially antialiases N contiguous horizontal pixels associated with M scanlines to generate a set of horizontally antialiased pixel data for the M scanlines. The horizontally antialiased pixel data for the M scanlines defines a set of vertically contiguous pixel data. The first and second storage units are capable of receiving and storing the horizontally antialiased pixel data associated with the M scanlines from the horizontal antialiasing unit. One storage unit receives and stores horizontally antialiased pixel data for the next M scanlines as a receiving buffer while the other storage unit provides the horizontally antialiased pixel data as an access buffer for vertical antialiasing. The vertical antialiasing unit is coupled to receive the horizontally-antialiased pixel data associated with the M scanlines from the access buffer. The vertical antialiasing unit performs vertical antialiasing on the vertically contiguous horizontally-antialiased pixel data to generate a pixel value for each NxM set of the high resolution pixel data.

In anther embodiment, the present invention provides a method for antialiasing a first set of pixel data of a first resolution into a second set of pixel data for display at the low resolution. The method includes: (a) sequentially receiving M consecutive scanlines of the first set of pixel data; (b) horizontally antialiasing N contiguous horizontal pixels for the M scanlines; (c) vertically antialiasing the horizontally antialiased pixel data on the M scanlines to generate antialiased pixel data for the M scanlines; (d) while vertically antialiasing the horizontally antialiased pixel data, sequentially receiving a next M consecutive scanlines of the first set of pixel data and horizontally antialiasing the pixel data of the next consecutive M scanlines; and (e) vertically antialiasing the pixel data of the next M scanlines to generate antialiased data for the next M scanlines.

In yet another embodiment, the present invention provides a device for antialiasing high resolution pixel data into low resolution pixel data for display at the low resolution. The high resolution pixel data defining pixel values for a plurality of horizontal scanlines with each scanline being defined by a plurality of the high resolution pixel data. The device includes means for sequentially receiving the high resolution pixel data and horizontal antialiasing means for sequentially antialiasing N contiguous horizontal pixels associated with M scanlines. The horizontal antialiasing means generates a set of horizontally antialiased pixel data for the M scanlines. The horizontally antialiased pixel data for the M scanlines defines a set of vertically contiguous pixel data. The device also includes first and second storing means for receiving and storing the horizontally antialiased pixel data associated with the M scanlines from the horizontal antialiasing unit. One storing means receives and stores horizontally antialiased pixel data for the next M scanlines as a receiving buffer while the other storing means provides the horizontally antialiased pixel data as an access buffer for vertical antialiasing. In addition, the device further includes vertical antialiasing means for performing vertical antialiasing on the vertically contiguous horizontally-antialiased pixel data to generate a pixel value for each NxM set of the high resolution pixel data.

Advantageously, the present invention generates antialiased pixel data at substantially real time rates with only M scanline delays. For example, storing M scanlines produces only M scanlines of delay in NxM antialiasing in contrast to conventional antialiasing techniques, which typically used an accumulation buffer that produced a delay of one or more frames. Moreover, the storage requirements are substantially smaller in that only M scanlines are stored as opposed to storing a whole frame of pixel data. Accordingly, the antialiasing device and method of the present invention provides an economical antialiasing solution with substantially real time performance. Furthermore, the antialiasing technique of the present invention allows users to recoup the cost of significant investment in their old, lower resolution monitors by allowing these monitors to run higher resolution applications. These and other advantages of the present invention will become apparent to those skilled in the art upon a study of the specification and drawings describing the present invention.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and form a part of this specification, illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.

Figure 1 illustrates a block diagram of an exemplary computer graphics system within which the present invention may be implemented or practiced.

Figure 2 shows a more detailed block diagram of a graphics subsystem in accordance with one embodiment of the present invention.

Figure 3 illustrates a more detailed block diagram of the graphics subsystem in accordance with another embodiment of the present invention.

Figure 4 illustrates a schematic block diagram of a pair of pixel scanlines for performing an exemplary 2x2 antialiasing.

Figure 5 illustrates a flow chart of an antialiasing method performed by an antialiasing unit in accordance with one embodiment of the present invention.

Figure 6 shows a schematic block diagram of the antialiasing unit for antialiasing input pixel data of resolution AxB into a lower (A/N)x(B/M) resolution for display at the lower resolution.

Figure 7 shows a schematic diagram of exemplary adders that may be used to implement horizontal and vertical antialiasing units in accordance with one embodiment of the present invention.

Figure 8 illustrates a timing diagram of a control unit in generating HSYNC2 and PCLK2 from HSYNC1 and PCLK2 for an exemplary 2x2 antialiasing.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention will now be described in detail with reference to exemplary preferred embodiments as illustrated in the accompanying drawings. In the following description, numerous specific details are set forth in order to provide a thorough understanding of the present invention. It will be apparent, however, to one skilled in the art, that the present invention can be practiced without some or all of these specific details. In other instances, well known process steps have not been described in detail in order not to unnecessarily obscure the present invention.

Figure 1 illustrates a block diagram of a computer graphics system 100 within which the present invention may be implemented or practiced. It should be appreciated that the computer graphics system 100 is exemplary only and that the present invention can operate within a number of different computer system configurations including general purpose computer systems, embedded computer systems, and computer systems specially adapted to electronic design automation. In describing various embodiments of the present invention, certain processes and operations are realized as a series of instructions (e.g., software programs) that reside within computer readable memory units of computer graphics system 100 and are executed by processors therein.

The computer graphics system 100 may be any computer-controlled graphics system suitable for generating 2D or 3D images. The computer graphics system 100 includes a bus 102 for transmitting digital information between the various parts of the computer system. One or more processors 104 for processing information are coupled to the bus 102. The information, together with the instructions for processing the information, are stored in a hierarchical memory system comprised of a mass storage device 108, a read only memory (ROM) 110, and a main memory 106. The mass storage device 108 is used to store a vast amount of data and may include one or more hard disk drives, floppy disk drives, optical disk drives, tape drives, CD-ROM drives, or any number of other types of storage devices having media for storing data digitally. The ROM 110 is used to store digital data on a permanent basis, such as instructions for the microprocessors. The main memory 106 is used for storing digital data on an intermediate basis. The main memory 106 can be DRAM, SDRAM, RDRAM, or any other suitable memory for storing data while the computer graphics system 100 is turned on.

The computer system 100 also includes a graphics subsystem 112 coupled to the bus 102 for processing graphics data. The processor 104 provides the graphics subsystem 112 with the

graphics data, such as drawing commands, coordinate vertex data, and other data related to an object's geometric position, color, texture, shading, and other surface parameters. From the graphics data provided, the graphics subsystem 112 generates high resolution graphics pixel data and converts the data into lower resolution data by antialiasing. The graphics unit 112 converts the lower resolution pixel data into video signals and transmits the signals to the display device 114. The display device 114 is coupled to the graphics subsystem 112 to receive graphics data for display at the lower resolution. Alternatively, the display device 114 may be coupled to the graphics system 100 via the bus 102 through a serial bus such as universal serial bus (USB) or IEEE 1394 bus.

Several other devices may also be coupled to the computer graphics system 100. For example, an alphanumeric keyboard 116 may be used for inputting commands and other information to processor 104 via the bus 102. A user input device such as a cursor control device 118 (e.g., a mouse, trackball, joystick, and touchpad) may be used for positioning a movable cursor and selecting objects on a computer screen.

Figure 2 shows a more detailed block diagram of the graphics subsystem 112 in accordance with one embodiment of the present invention. The graphics subsystem 112 includes a graphics processor 202, a frame buffer 204, an antialiasing unit 206, a digital-to-analog converter (DAC) 208, and a video amplifier 210. The graphics processor 202 receives graphics data and uses the frame buffer 204 in performing various well known graphics operations such as graphics transformation, scan conversion, rasterization to produce pixel values at a high resolution.

For example, the graphics processor 202 converts the graphical data into a screen coordinate system and may perform projection and transformation processes to generate graphics primitives such as points, lines, polygons, polyhedra, and the like. The graphics processor 102 may generate pixel data based on the received primitives by interpolating straight lines so that each intermediate value need not be individually and separately computed. The graphics processor 102 may also perform additional graphics functions such as Z-buffering, blending, and texturing on the pixel data. The resulting pixel data values (e.g., RGB values) are stored in the frame buffer 204. The graphics processor 102 may be implemented by using any suitable graphics processors such as Voodoo Banshee™ processor from 3dFx, Inc. of Santa Clara, California.

The pixel values are then transmitted to the antialiasing unit 206, which is coupled to the graphics processor 202. In addition to transmitting pixel data values, the graphics processor 202

also generates and transmits a horizontal sync signal HSYNC1, a vertical sync signal VSYNC1, and a pixel clock signal PCLK1 to the antialiasing unit 206. The horizontal sync signal HSYNC1 indicates the beginning of a new scan line while the vertical sync signal VSYNC1 specifies the top of an image frame. The pixel clock PCLK indicates each pixel in a horizontal scan line.

In accordance with one embodiment of the present invention, the antialiasing unit 206 performs NxM antialiasing on the received pixel data to generate a downscaled resolution adapted for display at a lower resolution in the display device 114 where N and M are integer numbers greater than 1. That is, the antialiasing unit takes NxM block of pixels to generate a single pixel value by determining an average pixel value. If, for example, the input pixel resolution per frame is AxB, then the output pixel resolution per frame is (A/N)x(B/M). In a preferred embodiment, the antialiasing unit 606 performs 2x2 antialiasing such that the resulting resolution is half the vertical and horizontal resolutions. For example, if the input resolution is 640x480, the antialiasing unit converts each of the 2x2 block of pixels in a pixel frame into a single pixel by determining the average of all four pixels in the 2x2 block to produce 320x240 output resolution. The generated pixel values are preferably in the form of red, green, and blue (RGB) pixel values. Preferably, A and B are integer multiples of N and M, respectively.

Display devices generally require synchronization signals VSYNC and HSYNC. To provide proper synchronization, the antialiasing unit 206 modifies HSYNC1 and PCKL1 signals to generate HSYNC2 and PCLK2, respectively. Specifically, the antialiasing unit 206 generates HSYNC2 at a pulse rate that is N times the sync rate of HSYNC1. For example, for 2x2 antialiasing, the pulse rate of HSYNC2 is half that of the HSYNC1. On the other hand, the antialiasing unit 206 generates VSYNC2 from VSYNC1 with a delay to account for the time delay in the antialiasing unit 206 to prevent skewing. The antialiasing unit 206 also clocks the pixel data through the antialiasing unit 206 to generate PCLK2 from PCLK1. The generated pixel data clock PCLK2 supports the pixel data rate of the display device 114. The antialiasing unit 206 outputs HSYNC2 and VSYNC2 to provide timing signals to the display device 114. For a CGA display device 114, the antialiasing unit 206 also generates a composite SYNC signal from the HSYNC2 and VSYNC2.

The DAC 208 is coupled to the antialiasing unit 206 to receive the pixel data and PCLK2 for converting the pixel data into analog RGB signals based on the pixel rate PCLK2. The video amplifier 210, which is optional and may be provided externally, is coupled to the DAC 208 to

receive the RGB signals and amplifies the RGB signals for transmission to the display device 114.

Figure 3 illustrates a more detailed block diagram of the graphics subsystem 112 in accordance with another embodiment of the present invention. The graphics subsystem 112 processes graphics data in a geometry unit 302, a scan conversion unit 304, and a rasterization unit 306. The geometry unit 302 converts the graphical data from the processor 104 into a screen coordinate system and may perform projection and transformation processes to give depth to a displayed object. The resulting primitives (points, lines, polygons, polyhedra, and the like) supplied by the geometry unit 302 are then provided to the scan conversion unit 304. The scan conversion unit 304 generates pixel data based on the received primitives by interpolating straight lines so that each intermediate value need not be individually and separately calculated by the geometry subsystem. The pixel data is then sent to the rasterization unit 306, where Z-buffering, blending, and texturing functions may be performed. The resulting pixel values are subsequently stored in the frame buffer 204 and transmitted to the antialiasing unit 206.

The antialising unit 206 receives the pixel data and performs antialiasing on NxM pixel blocks substantially in real time. Figure 4 illustrates a schematic block diagram of a pair of pixel scanlines (i.e., rows) for performing an exemplary 2x2 antialiasing. The illustrated scanlines 1 and 2 has an exemplary horizontal resolution of 640 pixels. The 2x2 horizontal antialiasing essentially takes a 2x2 block of pixels and generates a representative pixel from the four pixels in the block. For example, horizontal antialiasing takes a pair of consecutive pixels in scanline 1 and generates a single horizontally-antialiased pixel by averaging the pixel values. This is done for all the pixel pairs in the scanline 1 and scanline 2. Horizontal antialiasing thus generates 320 antialiased pixel values for each scanlines.

The 2x2 vertical antialiasing takes a pair of vertically contiguous pixel values that have been horizontally-antialiased and generates a single antialiased pixel by averaging the pixel values. For a vertical resolution of 480, this antialiasing scheme produces 320x240 resolution image. The quality of the resulting antialiased image as displayed on the display device 114 is superior to displaying a native 320x240 image because each of the antialiased pixel represents a sampling of a block of pixels. Even though 2x2 antialiasing scheme is illustrated herein, those skilled in the art will appreciate that the antialiasing unit 606 may employ any suitable NxM antialiasing scheme by antialiasing N consecutive pixels in horizontally and M consecutive horizontally-antialiased pixels vertically.

Figure 5 illustrates a flow chart of an antialiasing method performed by the antialiasing unit 206 in accordance with one embodiment of the present invention. In operation 502, the antialiasing unit 206 receives pixel data, HSYNC1, VSYNC1, and PCLK1 associated with pixel data. In operation 504, the antialiasing unit 206 sequentially performs horizontal antialiasing on blocks of N contiguous horizontal pixels for M consecutive scanlines to generate horizontally-antialiased pixel values. Specifically, N consecutive pixel data in a horizontal scanline forming a horizontal pixel block are summed and averaged to generate a single pixel value. The horizontal antialiasing thus compresses the pixels in the horizontal scanlines by the ratio 1/N to generate A/N number of pixel values for each scan line. The horizontal antialiasing is applied to each scanline in the set of M consecutive horizontal scanlines.

After horizontally antialiasing the set of M horizontal scanlines, it is determined whether more scanlines need to be received for antialiasing in operation 506. If so, the antialiasing unit 206 performs vertical antialiasing on the horizontally-antialiased pixel data in operation 512. While performing the vertical antialiasing of operation 512, the antialiasing unit 206 also receives pixel data for the next M consecutive scanlines along with HSYNC1, VSYNC1, and PCLK1 in operation 508 and performs horizontal antialiasing on the newly received pixel data in operation 510. After performing the vertical and horizontal operations, the method proceeds to generate HSYNC2 by dividing HSYNC1 by the ratio of input scanlines to output scanlines in operation 514. The method then proceeds back to operation 506 to determine whether more scanlines need to be received for antialiasing.

If no more scanlines need to be antialiased in operation 506, the method proceeds to operation 516, where the antialiasing unit 206 performs vertical antialiasing on the horizontally-antialiased pixel data on the M consecutive scanlines. From AxB resolution pixel data, the method thus generates (A/N)x(B/M) resolution pixels per frame for display. Then in operation 518, the antialiasing unit 206 generates a new vertical sync signal VSYNC2 by delaying VSYNC1. The method then terminates in operation 520.

Figure 6 shows a schematic block diagram of the antialiasing unit 206 for antialiasing input pixel data of resolution AxB into a lower (A/N)x(B/M) resolution for display at the lower resolution. The antialiasing unit 206 includes datapath circuitry 602, control unit 604, and a pair of storage units, RAM units A and B. The datapath circuitry 602 receives high resolution pixel data and is also coupled to transmit and receive control signals to and from the control unit 604 for performing antialiasing using the RAM units A and B. It should be appreciated that the

RAM units A and B may be implemented by employing any suitable RAM technology such as DRAM, SDRAM, SGRM, RDRAM, and the like.

The datapath circuitry 602 includes a horizontal antialiasing unit 610, a vertical antialiasing unit 612, a multiplexer 614, and a pair of buffers 616 and 618. The horizontal antialiasing unit 610 is coupled to the RAM units A and B through the buffers 616 and 618 for storing horizontally-antialiased pixel data. The horizontal antialiasing unit 610 sequentially receives the pixel data and performs horizontal antialiasing on a block of N contiguous horizontal pixels. Specifically, the horizontal antialiasing unit 610 determines and outputs an average of the N pixels as the horizontally-antialiased pixel value.

In one embodiment, the horizontal antialiasing unit 610 is implemented as one or more adders that add the N contiguous horizontal pixel values to determine the average of the pixels. For example, an adder can be used to add two 5-bit R pixel components to generate a 6-bit weighted sum, which corresponds to the average of the two 5-bit R components. Additionally, an adder may be implemented to add N pixel values by using various known weighting methods for each N pixel values. In a preferred embodiment, the adder sums two contiguous horizontal pixels to implement a 2x2 antialiasing scheme. Those skilled in the art will readily appreciate that an individual pixel data includes RGB components and as such, antialiasing may be performed on each R, G, and B components in parallel by using separate adders for each of the RGB components.

When N contiguous horizontal pixels have been horizontally-antialiased, the horizontally-antialiased pixel value (e.g., RGB values) is routed to RAM A for storage through a buffer 616. The control unit 604 asserts a buffer enable signal ENA to enable the buffer 616 and a write enable signal WEA to enable writing of the antialiased horizontal pixel value to the RAM unit A.

The vertical antialiasing unit 612 is coupled to the RAM units A and B to receive the stored horizontally-antialiased pixel values through the multiplexer 614. When the pixels of M horizontal scanlines have been received, horizontally-antialiased, and stored in the RAM unit A, the control unit 604 deasserts the buffer enable signal ENA and asserts a read enable signal REA to enable the vertical antialiasing unit 612 to access the stored horizontally-antialiased pixel values for vertical antialiasing. At the same time, the control unit generates a select signal SEL indicates that the RAM unit A is to be accessed for vertical antialiasing. The vertical antialiasing unit 612 then accesses and performs vertical antialiasing on the horizontally-

antialiased pixel data. The antialiased pixel data is then output to the DAC 208 for eventual display.

The vertical antialiasing unit 612, in one embodiment, is implemented as one or more adders, which add M vertically contiguous horizontally-antialiased pixels to determine the average of the pixels. For example, an adder can be used to add two 5-bit R pixel components to generate a 6-bit weighted sum, which corresponds to the average of the two 5-bit R components. In a preferred embodiment, the adder sums two contiguous vertical pixels to implement a 2x2 antialiasing scheme. Those skilled in the art will readily appreciate that an individual pixel data includes RGB components and as such, antialiasing may be performed on each R, G, and B components in parallel by using separate adders for each of the RGB components.

While the vertical antialiasing unit 612 is performing vertical antialiasing using the pixel data stored in RAM unit A, the horizontal antialiasing unit 610 sequentially receives next M scanlines and performs horizontal antialiasing. In order to store the horizontally-antialiased pixel data, the control unit 604 asserts a buffer enable signal ENB to enable the buffer 618 and a write enable signal WEB for RAM unit B. The signals ENB and WEB together allow the horizontal antialiasing unit to transfer the horizontally-antialiased pixel data to the RAM unit B for storage.

When the newly received M scanlines have been horizontally antialiased and stored in the RAM unit B, the vertical antialiasing unit 612 accesses RAM unit B while the horizontal antialiasing unit 602 received a next set of M scanlines for horizontal antialiasing and storage into RAM unit A. The control unit 604 generates the enable signals so as to alternate access to the RAM units A and B for the horizontal and vertical antialiasing units 602 and 612.

Figure 7 shows a schematic diagram of exemplary adders 702, 704, and 706 that may be used to implement the horizontal and vertical antialiasing units 610 and 612 in accordance with one embodiment of the present invention. In the illustrated embodiment, the adders 702, 704, and 706 are used to add two horizontally or vertically contiguous R, G, and B pixel data components, respectively, to generate a single antialiased output Rs, Gs, and Bs components, respectively. Each of the input R, G, and B components are of i-bit width. In a preferred embodiment, the output Rs, Gs, and Bs components are i+1 bit wide so that Rs, Gs, and Bs components represent antialiased values. Those skilled in the art will appreciate that the adders 702, 704, and 706 can be implemented to add N pixel components by employing various well known weighting techniques for each of the N pixel components.

Figure 8 illustrates a timing diagram of the control unit 604 in generating HSYNC2 and PCLK2 from HSYNC1 and PCLK2 for an exemplary 2x2 antialiasing. The input pixel data timing diagram 802, when asserted high, indicates when the input pixel data is received. The pixel data clock signal PCLK1 804 is generated at each pixel boundary. The signal HSYNC1 is deasserted when no input data is being received.

The control unit 604 generates HSYNC2 806 from HSYNC1 804 by doubling HSYNC1 804 to account for the fact that 2x2 antialiasing converts 2 contiguous pixel blocks into a single antialiased pixel. Preferably, a pulse width 812 of HSYNC2 806 is wider than a pulse width 810 of HSYNC1 to provide a greater synchronization margin. The control unit 604 also clocks the output pixel data 808 through the horizontal antialiasing unit 610 and generates PCLK2. The generated pixel data clock PCLK2 supports the pixel data rate of the display device 114 and is preferably double the rate of PCLK1.

In addition, the control unit 604 generates VSYNC2 from VSYNC1 with a delay to account for the time delay in the antialiasing unit 206 to prevent skewing. The control unit also generates multiplexer select signal SEL, buffer enable signals ENA and ENB, write enable signals WEA and WEB, and read enable signals REA and REB for controlling access to the RAM units A and B. The control unit 604 outputs HSYNC2 and VSYNC2 to provide timing signals to the display device 114. For a CGA display device 114, the antialiasing unit 206 also generates a composite SYNC signal by performing exclusive-OR function on signals HSYNC2 and VSYNC2.

The present invention thus antialiases pixel data at substantially real time rates with only M scanline delays. For example, the antialiasing unit 206 provides only 2 scanlines of delay in 2x2 antialiasing in contrast to conventional antialiasing techniques, which typically used an accumulation buffer that produced a delay of one or more frames. Moreover, the RAM units A and B are substantially smaller in that they store only M scanlines as opposed to storing a whole frame of pixel data. Accordingly, the antialiasing device and method of the present invention provides an economical antialiasing solution with substantially real time performance. Furthermore, the antialiasing technique of the present invention allows users to recoup the cost of significant investment in their old, lower resolution monitors by allowing these monitors to run higher resolution applications. The effects of antialiasing the high resolution pixel image into the lower resolution pixel image may be adequate for many applications such as video games.

While this invention has been described in terms of several preferred embodiments, there are alterations, permutations, and equivalents which fall within the scope of this invention. It should also be noted that there are alternative ways of implementing both the methods and devices of the present invention. It is therefore intended that the following appended claims be interpreted as including all such alterations, permutations, and equivalents as fall within the true spirit and scope of the present invention.

CLAIMS

What is claimed is:

1. A device for antialiasing high resolution pixel data into low resolution pixel data for display at the low resolution, the high resolution pixel data defining pixel values for a plurality of horizontal scanlines, each scanline being defined by a plurality of the high resolution pixel data, the device comprising:

a horizontal antialiasing unit adapted to sequentially receive the high resolution pixel data, the horizontal antialiasing unit sequentially antialiasing N contiguous horizontal pixels associated with M scanlines to generate a set of horizontally antialiased pixel data for the M scanlines, the horizontally antialiased pixel data for the M scanlines defining a set of vertically contiguous pixel data;

a first storage unit and a second storage unit capable of receiving and storing the horizontally antialiased pixel data associated with the M scanlines from the horizontal antialiasing unit, one storage unit receiving and storing horizontally antialiased pixel data for the next M scanlines as a receiving buffer while the other storage unit provides the horizontally antialiased pixel data as an access buffer for vertical antialiasing; and

a vertical antialiasing unit coupled to receive the horizontally-antialiased pixel data associated with the M scanlines from the access buffer for performing vertical antialiasing on the vertically contiguous horizontally-antialiased pixel data to generate a pixel value for each NxM set of the high resolution pixel data.

2. The device as recited in claims 1, wherein the first and second storage units alternate as the receiving buffer and the access buffer.

3. The device as recited in claim 1, further comprising:

a multiplexer coupled between the vertical antialiasing unit and the first and second storage units for transmitting the horizontally antialiased pixel data from the access buffer to the vertical antialiasing unit.

4. The device as recited in claim 1, wherein N and M are 2 to implement 2x2 antialiasing.

5. The device as recited in claim 1, wherein the high resolution is AxB and the low resolution is (A/N)x(B/M).

6. The device as recited in claim 1, further comprising:

a first buffer coupled between the horizontal antialiasing unit and the first storage unit, the first buffer buffering the horizontally antialiased pixel data for storage in the first storage unit when the first storage unit is the receiving buffer; and

a second buffer coupled between the horizontal antialiasing unit and the first storage unit, the first buffer buffering the horizontally antialiased pixel data storage in the second storage unit when the second storage unit is the receiving buffer.

7. The device as recited in claim 1, further comprising:

a control unit coupled to the first and second storage units and being arranged to select one storage unit as the receiving buffer and the other storage unit as the access buffer.

8. The device as recited in claim 1, wherein the pixel data includes R, G, and B components for each pixel.

9. The device as recited in claim 8, wherein the horizontal and vertical antialiasing units perform antialiasing on each of the R, G, and B components.

10. The device as recited in claim 1, wherein the horizontal and vertical antialiasing units include one or more adders.

11. The device as recited in claim 1, wherein the horizontal and vertical antialiasing convert a set of contiguous NxM pixels into a single pixel.

12. A method for antialiasing a first set of pixel data of a first resolution into a second set of pixel data for display at the low resolution, the method comprising:

a) sequentially receiving M consecutive scanlines of the first set of pixel data;

b) horizontally antialiasing N contiguous horizontal pixels for the M scanlines;

c) vertically antialiasing the horizontally antialiased pixel data on the M scanlines to generate antialiased pixel data for the M scanlines;

d) while vertically antialiasing the horizontally antialiased pixel data, sequentially receiving a next M consecutive scanlines of the first set of pixel data and horizontally antialiasing the pixel data of the next consecutive M scanlines; and

e) vertically antialiasing the pixel data of the next M scanlines to generate antialiased data for the next M scanlines.

13. The method as recited in claim 12, wherein the first resolution is higher than the second resolution.

14. The method as recited in claim 12, wherein the first resolution is AxB and the second resolution is (A/N)x(B/M).

15. The method as recited in claim 12, wherein the horizontal antialiasing includes determining an average pixel value for the N contiguous pixels.

16. The method as recited in claim 12, wherein the vertical antialiasing includes determining an average pixel value for the horizontally antialiased pixel data.

17. The method as recited in claim 12, wherein N and M are 2 to implement 2x2 antialiasing.

18. The method as recited in claim 12, wherein the pixel data includes R, G, and B components for each pixel.

19. The device as recited in claim 18, wherein each of the R, G, and B components of a pixel value is antialiased.

20. The device as recited in claim 1, wherein the horizontal antialiasing operation adds N contiguous pixel data.

21. The device as recited in claim 1, wherein the horizontal and vertical antialiasing converts a set of contiguous NxM pixels into a single pixel.

22. A device for antialiasing high resolution pixel data into low resolution pixel data for display at the low resolution, the high resolution pixel data defining pixel values for a plurality of horizontal scanlines, each scanline being defined by a plurality of the high resolution pixel data, the device comprising:

means for sequentially receiving the high resolution pixel data;

horizontal antialiasing means for sequentially antialiasing N contiguous horizontal pixels associated with M scanlines to generate a set of horizontally antialiased pixel data for the M scanlines, the horizontally antialiased pixel data for the M scanlines defining a set of vertically contiguous pixel data;

first storing means and second storing means for receiving and storing the horizontally antialiased pixel data associated with the M scanlines from the horizontal antialiasing unit, one storing means receiving and storing horizontally antialiased pixel data for the next M scanlines as a receiving buffer while the other storing means provides the horizontally antialiased pixel data as an access buffer for vertical antialiasing; and

vertical antialiasing means for performing vertical antialiasing on the vertically contiguous horizontally-antialiased pixel data to generate a pixel value for each NxM set of the high resolution pixel data.

23. The device as recited in claims 22, wherein the first and second storing means alternate as the receiving buffer and the access buffer.

24. The device as recited in claim 23, further comprising:

multiplexing means for transmitting the horizontally antialiased pixel data from the access buffer to the vertical antialiasing unit.

25. The device as recited in claim 22, wherein N and M are 2 to implement 2x2 antialiasing.

26. The device as recited in claim 22, wherein the high resolution is AxB and the low resolution is (A/N)x(B/M).

27. The device as recited in claim 22, further comprising:

a control unit for selecting one of the storing means as the receiving buffer and the other storing means as the access buffer.

28. The device as recited in claim 22, wherein the pixel data includes R, G, and B components for each pixel.

29. The device as recited in claim 28, wherein the horizontal and vertical antialiasing units perform antialiasing on each of the R, G, and B components.

30. The device as recited in claim 22, wherein the horizontal and vertical antialiasing means include one or more adders.

32. The device as recited in claim 22, wherein the horizontal and vertical antialiasing means convert a set of contiguous NxM pixels into a single pixel.

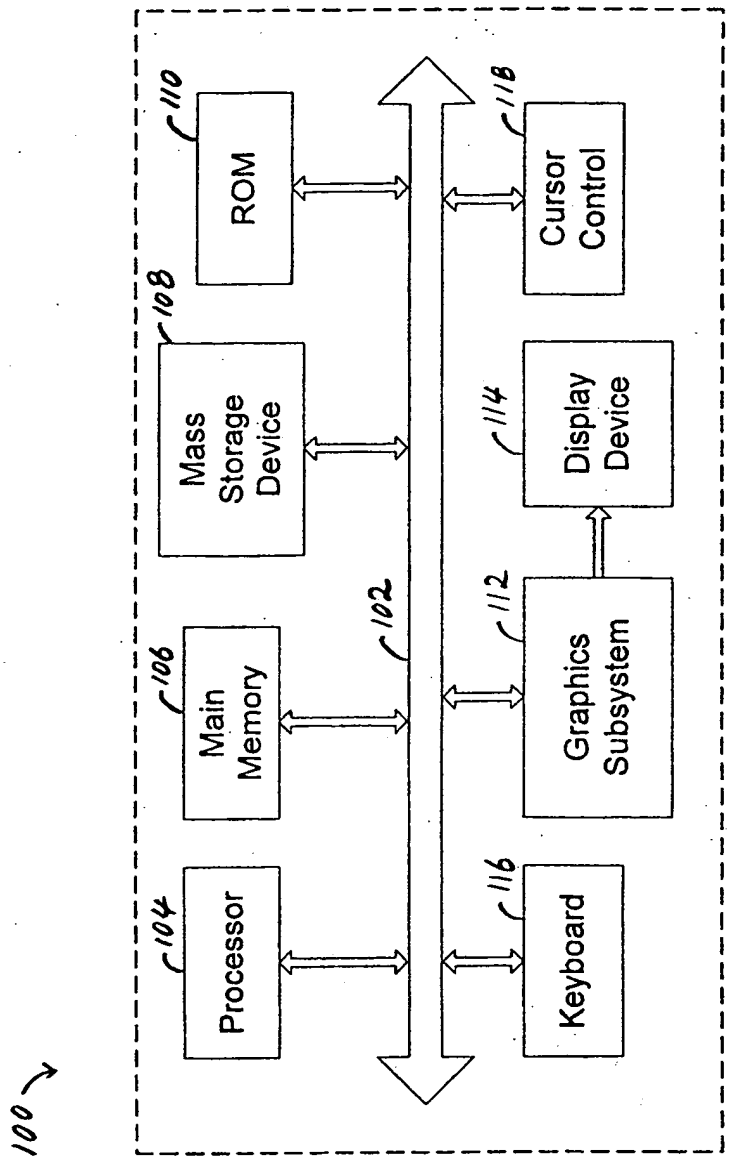
100
110
ROM
108
Mass Storage Device
106
Main Memory
104
Processor
102
118
Cursor Control
114
Display Device
112
Graphics Subsystem
116
Keyboard

FIG. 1

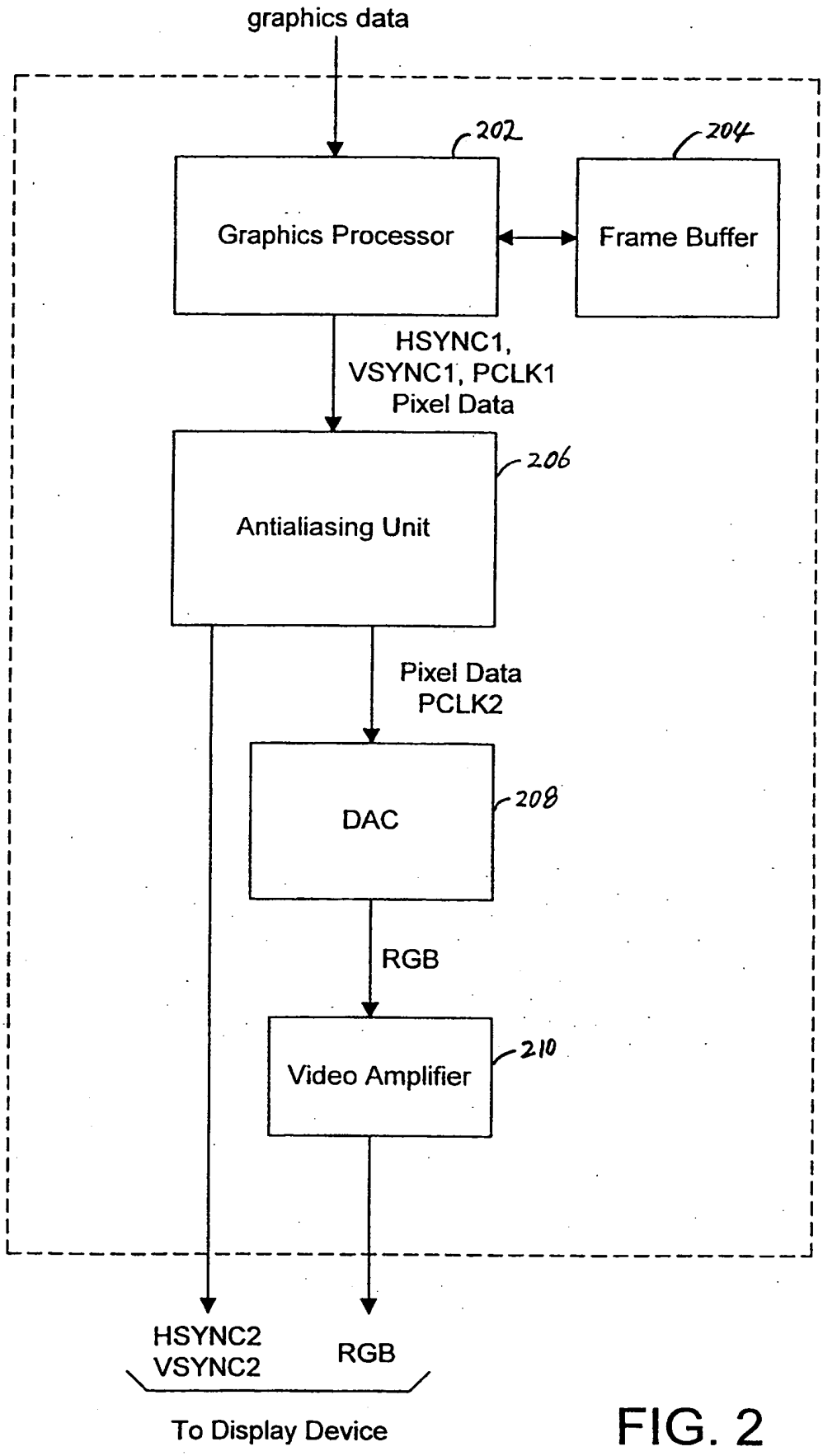
graphics data
202
204
Graphics Processor
Frame Buffer
HSYNC1,
VSYNC1, PCLK1
Pixel Data
206
Antialiasing Unit
Pixel Data
PCLK2
DAC
208
RGB
Video Amplifier
210
HSYNC2
VSYNC2
RGB
To Display Device

FIG. 2

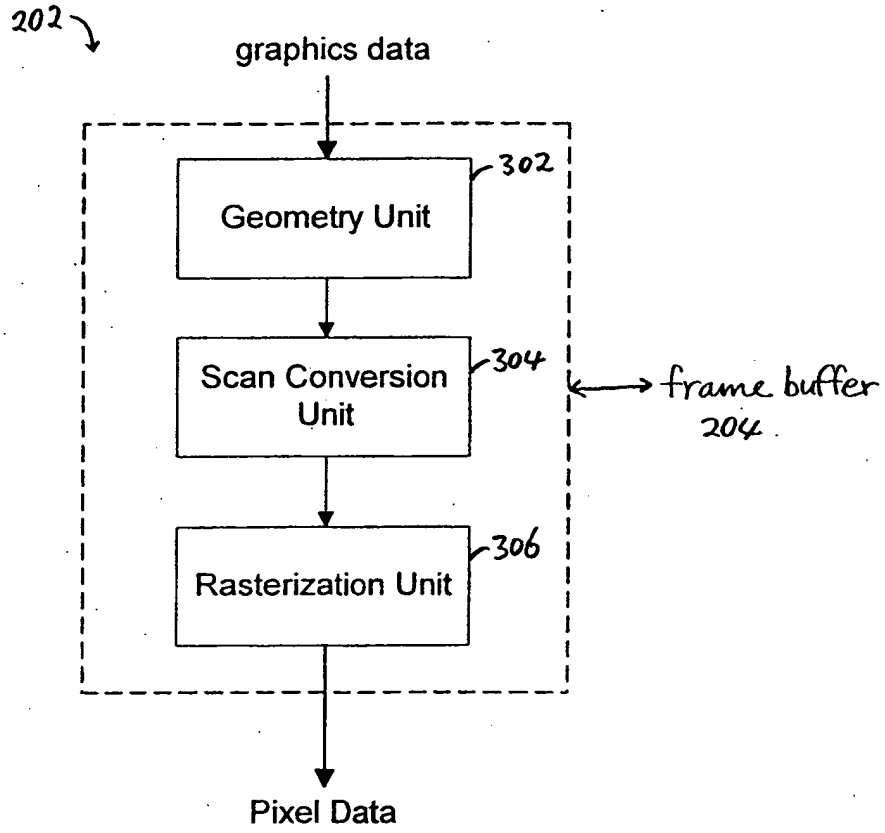
202
graphics data
Geometry Unit
302
Scan Conversion Unit
304
frame buffer 204
Rasterization Unit
306
Pixel Data

FIG. 3

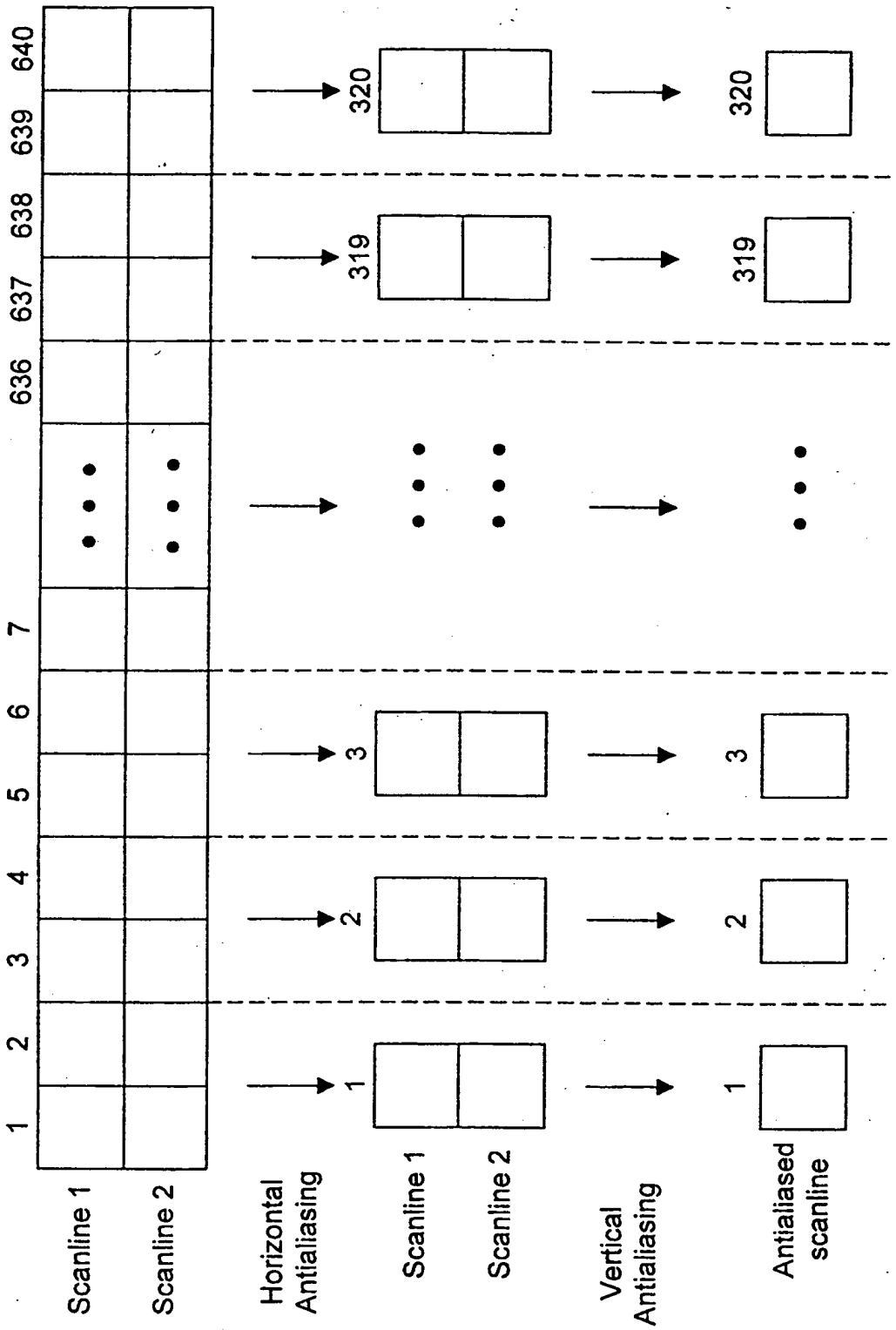
Scanline 1
Scanline 2
Horizontal Antialiasing
Scanline 1
Scanline 2
Vertical Antialiasing
Antialiased scanline
1
2
3
4
5
6
7
636
637
638
639
640
1
2
3
319
320

FIG. 4

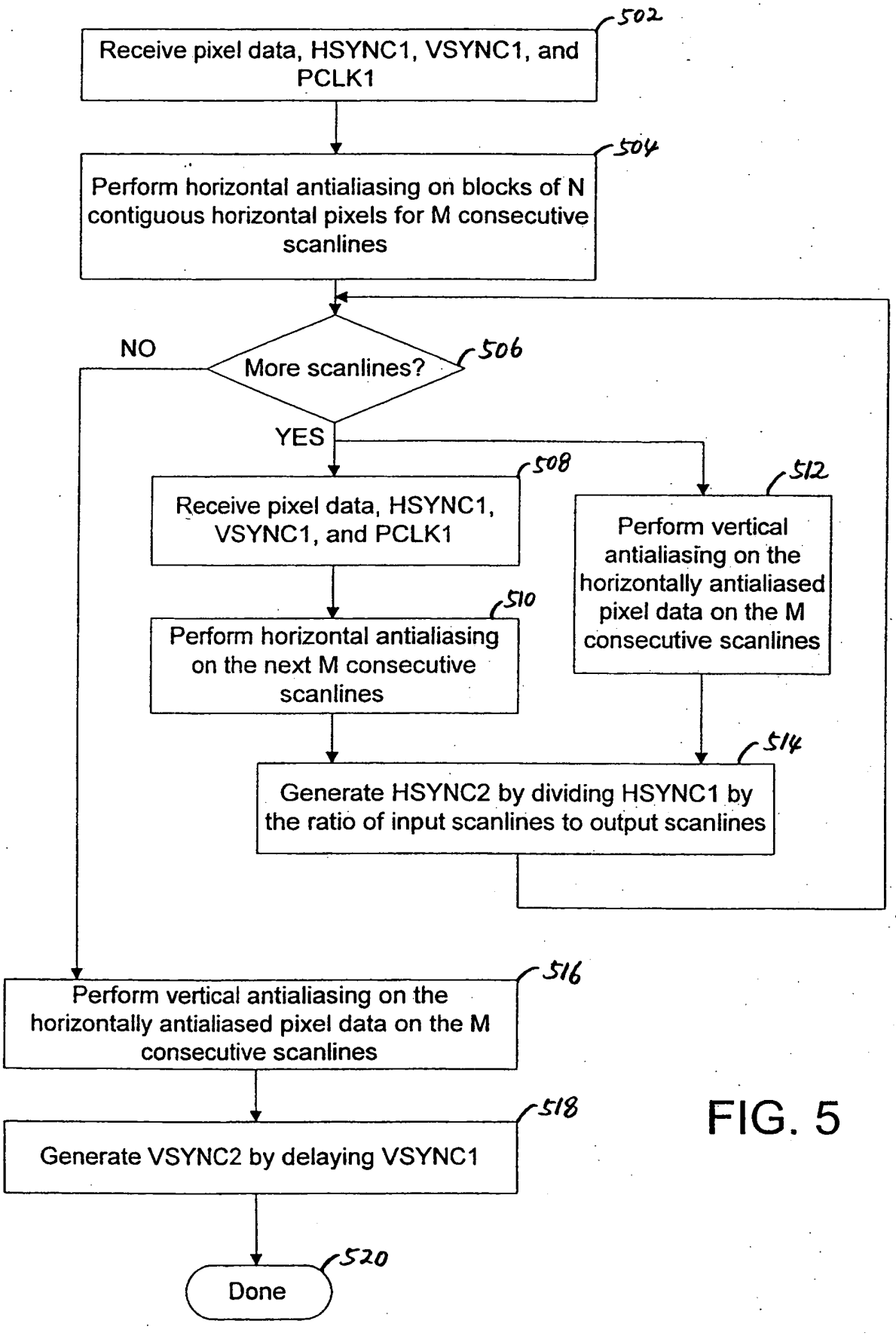
502
Receive pixel data, HSYNC1, VSYNC1, and PCLK1
504
Perform horizontal antialiasing on blocks of N contiguous horizontal pixels for M consecutive scanlines
NO
More scanlines?
506
YES
508
Receive pixel data, HSYNC1, VSYNC1, and PCLK1
510
Perform horizontal antialiasing on the next M consecutive scanlines
512
Perform vertical antialiasing on the horizontally antialiased pixel data on the M consecutive scanlines
514
Generate HSYNC2 by dividing HSYNC1 by the ratio of input scanlines to output scanlines
516
Perform vertical antialiasing on the horizontally antialiased pixel data on the M consecutive scanlines
518
Generate VSYNC2 by delaying VSYNC1
520
Done

FIG. 5

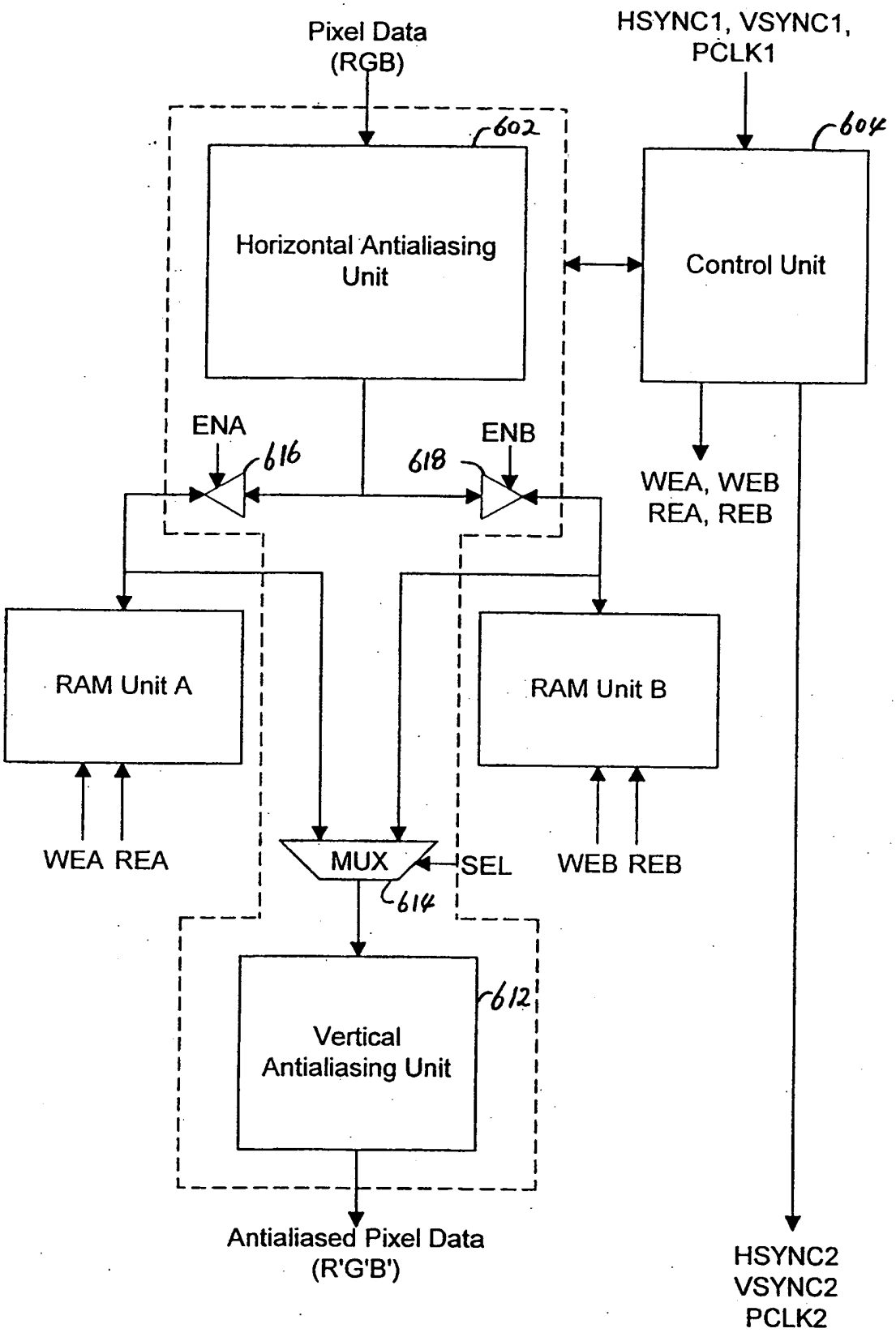
Pixel Data
(RGB)
HSYNC1, VSYNC1,
PCLK1
602
604
Horizontal Antialiasing
Unit
Control Unit
ENA
616
618
ENB
WEA, WEB
REA, REB
RAM Unit A
RAM Unit B
WEA REA
MUX
SEL
WEB REB
614
612
Vertical
Antialiasing Unit
Antialiased Pixel Data
(R'G'B')
HSYNC2
VSYNC2
PCLK2

FIG. 6

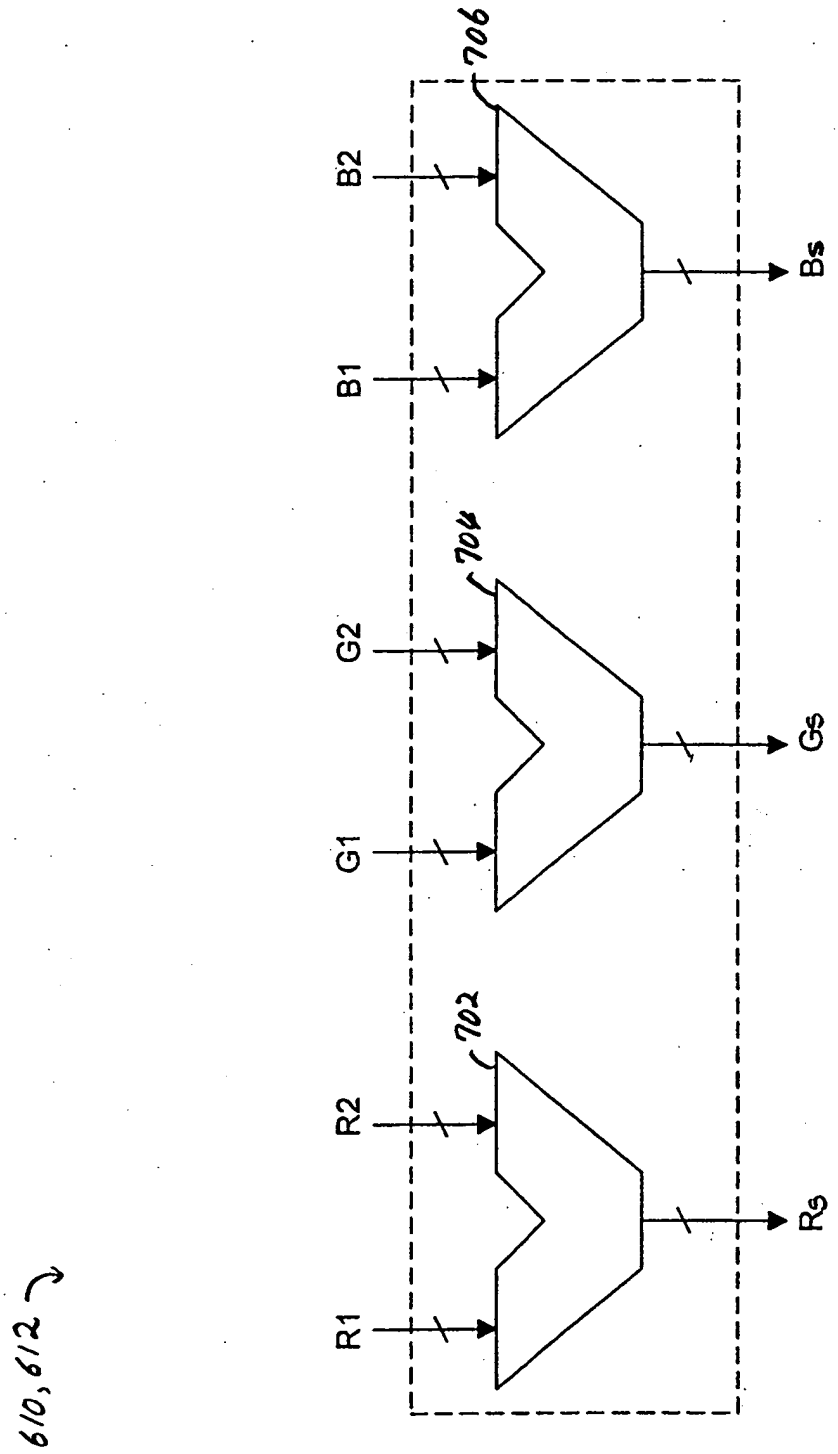

FIG. 7

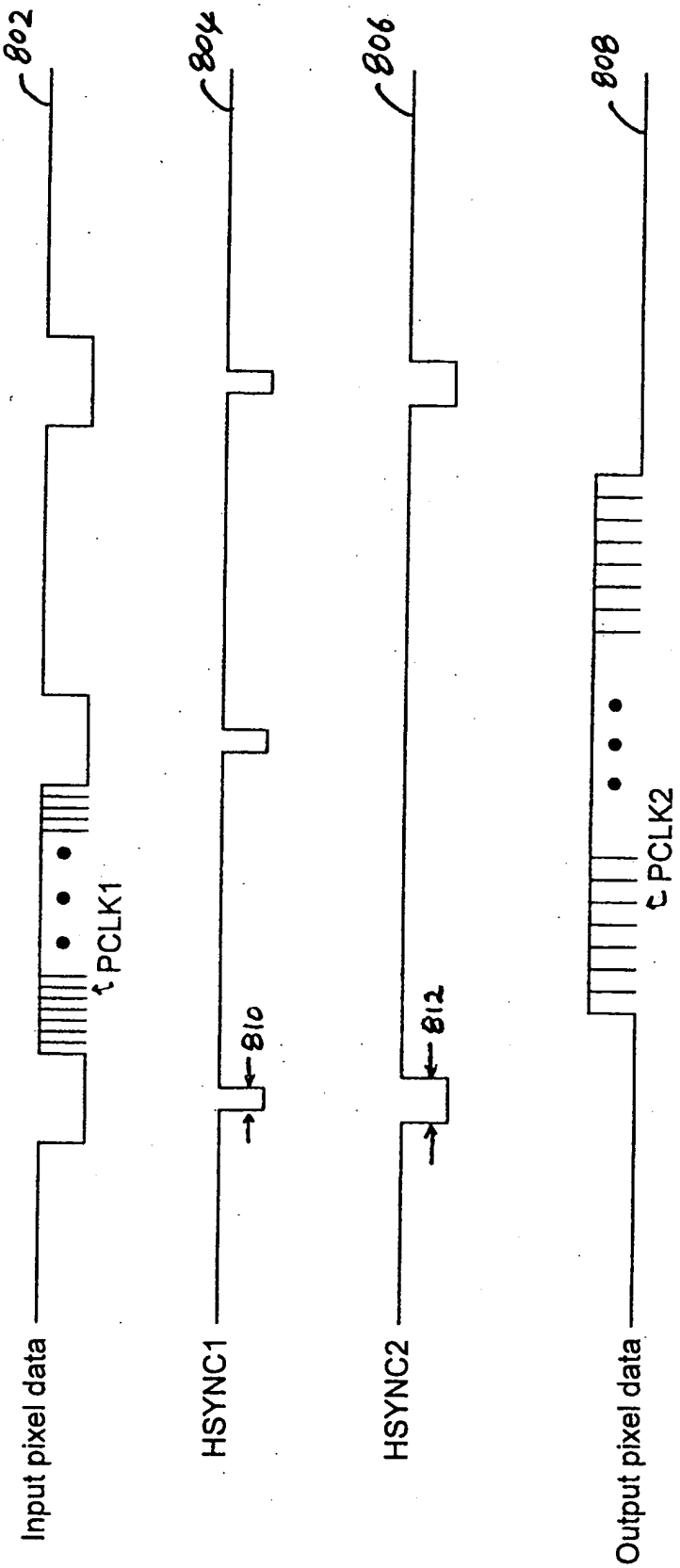
802
804
806
808
PCLK1
PCLK2
810
812
Input pixel data
HSYNC1
HSYNC2
Output pixel data

FIG. 8

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INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 7 : G09G 5/36, G06T 11/20

A3

(11) International Publication Number: **WO 00/30033**

(43) International Publication Date: 25 May 2000 (25.05.00)

(21) International Application Number: PCT/US99/27449

(22) International Filing Date: 17 November 1999 (17.11.99)

(30) Priority Data:
60/108,784 17 November 1998 (17.11.98) US

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(81) Designated States: AE, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CR, CU, CZ, DE, DK, DM, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).

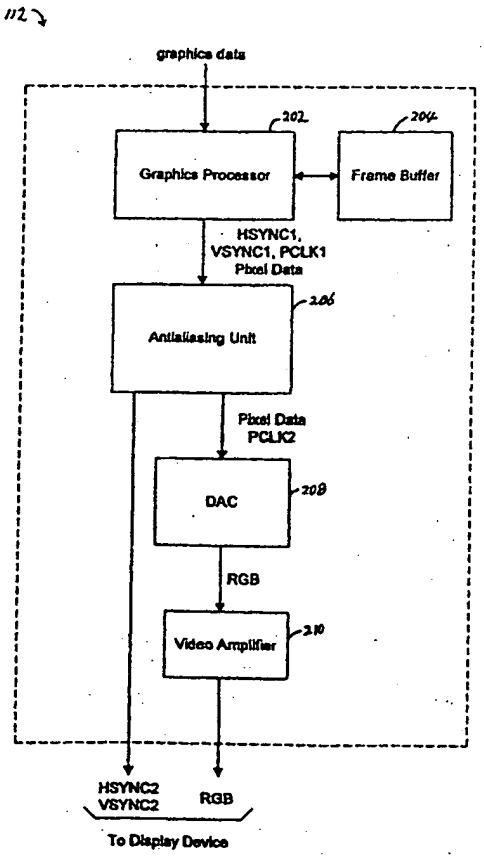
Published
With international search report.

(88) Date of publication of the international search report:
20 July 2000 (20.07.00)

(54) Title: DEVICE AND METHOD FOR ANTIALIASING HIGH RESOLUTION PIXEL DATA FOR LOWER RESOLUTION DISPLAY

(57) Abstract

Disclosed is a device and a method for antialiasing high resolution pixel data into low resolution pixel data for display at the low resolution. Figure 2 shows a detailed block diagram of the graphics subsystem (112) in accordance with one embodiment of the present invention. The graphics subsystem (112) includes: a graphics processor (202), which generates HSYNC1, VSYNC1, PCLK1 Pixel Data, a frame buffer (204) that transmits pixel data values, to the graphics processor (202) and an antialiasing unit (206), coupled to the graphics processor (202). The antialiasing unit (206) transmits HSYNC2 and VSYNC2 to the display device. The DAC (208) receives pixel data PCLK2 from the antialiasing unit (206) and transmits RGB to the video amplifier (210), which is optinal and may be provided externally. The video amplifier drives the RGB to the display device.



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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US99/27449

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :G09G 5/36, G06T 11/20
US CL :345/136, 441, 443

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 345/136, 441, 443

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

Please See Extra Sheet.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5,299,300 A (FEMAL et al) 29 MARCH 1994, figs 1-2, 4, and 14-17, abstract, lines 1-18, col. 1, lines 64-68, col. 2, lines 1-40	1-3, 5-9, 12-16, 18-20, 22-24, and 26-29
Y	US 5,598,184 A (BARKANS) 28 January 1997, figs. 6-8, 12-17, and 23	4, 6, 10-11, 17, 21, 25, and 30-31
Y	US 5,596,684 A (OGLETREE et al) 21 January 1997, figs. 9a-10b	1, 12, and 22
Y	US 5,742,277 A (GOSSETT et al) 21 April 1998, figs. 9a-9b, 12a-12i	4, 6, 17, 21, 25, and 30-31

[X] Further documents are listed in the continuation of Box C. [ ] See patent family annex.

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US99/27449

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US 5,742,277 A (GOSSETT et al) 21 April 1998, figs. 1, 4-7, and 10-11, col. 4, lines 33-67, col. 5, lines 1-51	2-3, 5, 7-11, 18-20, and 26-29

INTERNATIONAL SEARCH REPORT

International application No.
PCT/US99/27449

B. FIELDS SEARCHED

Electronic data bases consulted (Name of data base and where practicable terms used):

STN , USPTO DATABASE

serch terms: antialiasing, DAC, low resoultion and high resolution, low resolution display, vertical, horizontal, scanlines, and inventor search